

ABSTRACT OF THE DISCLOSURE

Method, system and computer-executable code are disclosed for synthesizing a representation of a circuit into a new circuit representation having greater unateness. The invention includes partitioning a circuit representation to obtain a representation of at least one sub-circuit, recursively decomposing the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit, merging the sum-of-products or product-of-sums representation into the circuit representation to form a new circuit representation, and repeating until a desired level of unateness for the new circuit representation is achieved.

Algebraic division is implemented to merge common expressions of the sum-of-products or product-of-sums representations. A zero-suppressed binary decision diagram is implemented to recursively decompose the representation of the sub-circuit.

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